CofC

ATTORNEY'S DOCKET NO.: S1022.80719US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sebastien Ferroussat	
Serial No.:	09/919,482	Patent No. 6,983,300 B2
Filed:	July 30, 2001	Issued: January 3, 2006
For:	ARITHMETIC UNIT	
Examiner:	David H. Malzahn	
Art Unit:	2193	Confirmation No.: 3921

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.323

Sir/Madam:

Patentee respectfully requests the correction of errors found in the above-captioned patent. Specifically, the residence of the inventor is incorrect and there is an error of omission in claim 26 of issued U.S. Patent No. 6,983,300 B2.

The inventor's residence should read "Anberieu En Bugey, France" as shown on the Declaration and Power of Attorney not "Fontaine, France" as is shown on the title page of U.S. Patent No. 6,983,300.

Claim 26 as found in issued in column 10 of U.S. Patent No. 6,983,300 is reproduced below:

> 26. An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:
> an input for receiving said plurality of values;
> an adder for adding said values to define a result, wherein said adder comprises a plurality of 3 to 2 carry save adders, said result being within a first range -2^N to 2^N-1;
> circuitry for performing a round on the result to define a rounded result, wherein the rounded result falls within a third range -2^N **to** $2^N-1+2^{(N/2)-}$;
> a detector for determining if said result falls within a second range -2^N to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and
> circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range. (Emphasis added)

JAN 18 2006

Claim 49 as filed (claim 26 in issued US Patent No. 6,983,300) is reproduced below:

> 49. An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:
> an input for receiving said plurality of values;
> an adder for adding said values to define a result, wherein said adder comprises a plurality of 3 to 2 carry save adders, said result being within a first range -2^N to 2^N-1;
> circuitry for performing a round on the result to define a rounded result, wherein the rounded result falls within a third range **-2^N to $2^N-1+2^{(N/2)-1}$**;
> a detector for determining if said result falls within a second range -2^N to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and
> circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range. (Emphasis added)

No amendment was made by the Examiner or Patentee to change the equation "-2^N to $2^N-1+2^{(N/2)-1}$" to "-2^N to $2^N-1+2^{(N/2)-}$" in claim 26, column 10, line 29 of US. patent No. .6.983,300. That is, the final figure "1" should not have been removed from the equation.

In support of the above, Patentee encloses a highlighted copy of the Declaration and Power of Attorney; page 7 of the amendment filed on April 4, 2005 and the title page and column 10 of issued U.S. Patent No. 6,983,300. Also enclosed is a Certificate of Correction form PTO Form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Since neither of the above amendments were made by either Patentee or the Examiner it is respectfully requested that the corrections as specified herein and on the attached Certificate of Correction, PTO form SB/44 be made and a Certificate of Correction be granted. Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 9nd day of January, 2006.

Gail Driscoll

Attorney Docket No.: S1022.80719US00
XNDD

Respectfully submitted,

Sebastien Ferroussat, Applicant

By: _____

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600 Atlantic Avenue
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Tel. (617) 646.8000

DOCKET NO.: S1022.80719US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sebastien Ferroussat	
Serial No.:	09/919,482	Patent No. 6,983,300 B2
Filed:	July 30, 2001	Issued: January 3, 2006
For:	ARITHMETIC UNIT	
Examiner:	David H. Malzahn	
Art Unit:	2193	Confirmation No.: 3921

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Dec; Page 7 of 04/04/05 Amn, Title Page and Col 10 of U.S. Pat No. 6,983,300.
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646.8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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By:

Attorney Docket No.: S1022.80719US00
XNDD

Respectfully submitted,

Sebastien Ferroussat, Applicant

James H. Morris, Reg. No.: 34,681
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Boston, Massachusetts 02210
Tel. (617) 646.8000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sebastien Ferroussat	
Serial No.:	09/919,482	Patent No. 6,983,300 B2
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ATTN: Certificate of Correction Branch
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Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: De c; Page 7 of 04/04/05 Amn, Title Page and Col 10 of U.S. Pat No. 6,983,300.
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If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646.8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 9nd day of January, 2006.

By:

Respectfully submitted,

Sebastien Ferroussat, Applicant

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600 Atlantic Avenue
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Tel. (617) 646.8000

Attorney Docket No.: S1022.80719US00
XNDD

US006983300B2

(12) **United States Patent**
Ferroussat

(10) **Patent No.: US 6,983,300 B2**
(45) **Date of Patent: Jan. 3, 2006**

(54) **ARITHMETIC UNIT**

(75) Inventor: **Sebastien Ferroussat**, Fontaine (FR)

(73) Assignee: **STMicroelectronics S.A.**, Gentilly (FR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 715 days.

(21) Appl. No.: **09/919,482**

(22) Filed: **Jul. 30, 2001**

(65) **Prior Publication Data**

US 2002/0038202 A1 Mar. 28, 2002

(30) **Foreign Application Priority Data**

Aug. 1, 2000 (EP) 00410091

(51) **Int. Cl.**
G06F 7/50 (2006.01)

(52) **U.S. Cl.** **708/552**; 708/553

(58) **Field of Classification Search** 708/551–553, 708/497–498

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,164,914	A *	11/1992	Anderson	708/552
5,677,860	A *	10/1997	Yazawa et al.	708/552
2002/0103842	A1 *	8/2002	Goldovsky	708/552

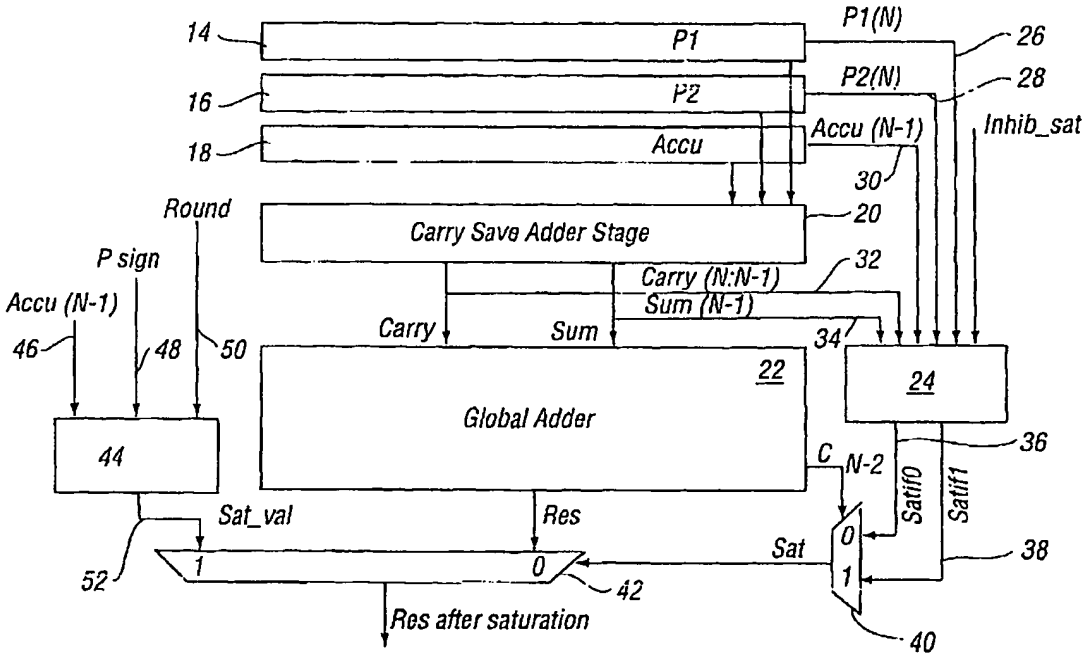
* cited by examiner

Primary Examiner—D. H. Malzahn
(74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; James H. Morris; Wolf, Greenfield & Sacks, P.C.

(57) **ABSTRACT**

An arithmetic unit for adding a plurality of values to define a result, the arithmetic unit including circuitry for receiving the plurality of values; circuitry for adding the plurality of values to define a result, the result being within a first range; circuitry for determining if the result falls within a second range, the second range being smaller than the first range, the circuitry arranged to consider only some of the bits of the result; and circuitry for modifying the result in so that the result output by said arithmetic unit falls within the second range.

26 Claims, 3 Drawing Sheets



to the sign of the total of a first and a second value and information as to one bit of a third value to determine if the result can fall out of said second range at the positive end thereof or the negative end thereof.

20. A unit as claimed in claim **1**, wherein said plurality of values comprise a plurality of partial products.

21. A unit as claimed in claim **1**, wherein said plurality of values comprise an accumulator.

22. A unit as claimed in claim **1**, wherein a plurality of registers are provided for storing said plurality of values.

23. An arithmetic unit for adding three values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said values;

an adder for adding said values to define a result, said result being within a first range -2^N to 2^N-1;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the first range, said detector being arranged to consider only some bits of said result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

24. An arithmetic unit for adding three values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said values;

an adder for adding said values to define a result, said result being within a first range -2^N to 2^N-1;

circuitry for performing a round on the result, to define a rounded result, wherein the rounded result falls within a third range -2^N to $2^N-1+2^{(N/2)-1}$;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and

circuitry for modifying said rounded result in so that the result output by said arithmetic unit falls within the second range.

25. An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said values to define a result, wherein said adder comprises a carry save adder stage comprising a plurality of 3 to 2 carry save adders, said result being within a first range -2^N to 2^N-1;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the first range, said detector being arranged to consider only some bits of said result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

26. An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said values to define a result, wherein said adder comprises a plurality of 3 to 2 carry save adders, said result being within a first range -2^N to 2^N-1;

circuitry for performing a round on the result to define a rounded result, wherein the rounded result falls within a third range -2^N to $2^N-1+2^{(N/2)-}$;

a detector for determining if said result falls within a second range -2^N to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

* * * * *

48. (New) An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said values to define a result, wherein said adder comprises a carry save adder stage comprising a plurality of 3 to 2 carry save adders, said result being within a first range -2^{N} to $2^{N}-1$;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the first range, said detector being arranged to consider only some bits of said result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

49. (New) An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said values to define a result, wherein said adder comprises a plurality of 3 to 2 carry save adders, said result being within a first range -2^{N} to $2^{N}-1$;

circuitry for performing a round on the result to define a rounded result, wherein the rounded result falls within a third range -2^{N} to $2^{N}-1+2^{(N/2)-1}$;

a detector for determining if said result falls within a second range -2^{N} to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

Attorney's Docket No. S1022/8719

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled ARITHMETIC UNIT the specification of which was filed on July 30, 2001, as United States Application No. 09/919,482, bearing attorney docket No. S1022/8719.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or section 365(a) of any PCT International application designating at least one country other than the United States listed below and have also identified below any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign PCT International Application(s)and any priority claims under 35 U.S.C. §§119 and 365(a),(b):

			Priority Claimed
00410091.3	Europe	1 August 2000 (01.08.00)	☒ ☐
(Number)	(Country-if PCT, so indicate)	(DD/MM/YY Filed)	YES NO
			☐ ☐
(Number)	(Country)	(DD/MM/YY Filed)	YES NO
			☐ ☐
(Number)	(Country-if PCT, so indicate)	(DD/MM/YY Filed)	YES NO

I am the inventor of European application number 00410091.3, filed August 1, 2000, which application was filed by the assignee STMicroelectronics, S.A.

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

(Application Number) (filing date)

(Application Number) (filing date)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT International application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

JAN 18 2006

(Application No.) (filing date) (status-patented, pending, abandoned)

(Application No.) (filing date) (status-patented, pending, abandoned)

PCT International Applications designating the United States:

(PCT Appl. No.) (U.S. Ser. No.) (PCT filing date) (status-patented,pending,abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David Wolf	17,528	Peter C. Lando	34,654	Matthew B. Lowrie	36,904	Daniel P. McLoughlin	46,066
George L. Greenfield	17,756	Gary S. Engelson	35,128	Robert A. Skrivanek, Jr.	40,886	Robert H. Walat	46,324
Stanley Sacks	19,900	Randy J. Pritzker	35,986	Robert M. Abrahamsen	37,482	Thomas G. Field	45,596
Edward F. Perlman	28,105	Richard F. Giunta	36,149	Edward J. Russavage	43,069	Michael J. Pomianek	46,190
Lawrence M. Green	29,384	Douglas R. Wolf	36,971	Neil P. Ferraro	39,188	M. Brad Lawrence	47,210
Steven J. Henry	27,900	Elizabeth R. Plumer	36,637	Lisa E. Winsor	44,405	Theodore E. Galanthay	24,122
Edward R. Gates	31,616	Timothy J. Oyer	36,628	Mark Steinberg	40,829	Lisa K. Jorgenson	34,845
William R. McClellan	29,409	John N. Anastasi	37,765	Stephen R. Finch	42,534	Robert D. McCutcheon	38,717
Ronald J. Krandsdorf	20,004	Helen C. Lockhart	39,248	Joseph Teja, Jr.	45,157	Mario J. Donato, Jr.	37,816
Jason M. Honeyman	31,624	James M. Hanifin, Jr.	37,929	Jeffrey B. Powers	45,021	Nainesh Shah	40,166
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c/o Wolf, Greenfield & Sacks, P.C.,
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600 Atlantic Avenue
Boston, MA 02210-2211

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's signature Sebastien Ferroussat Date 20 September 2001
Full name of sole or first inventor Sebastien Ferroussat
Citizenship ~~United States of America~~ FRANCE
Residence ~~81 Avenue Aristide Briand, 38600 Fontaine, France~~
Post Office Address ~~81 Avenue Aristide Briand, 38600 Fontaine, France~~ | 5 RUE ANDRE LEMITRE 01500 AMBERIEU EN BUGEY FRANCE.

JAN 18 2006

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PTO/SB/44 (04-04)
Approved for use through 04/30/2007
U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,983,300
DATED	:	January 3, 2006
INVENTOR(S)	:	Sebastien Ferroussat

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item (75) should read as shown below:

(75) Inventor: Sevastien Ferroussat, Anberieu En Bugey, France

Claim 26, col. 10, line 53 should read as shown below:
--a third range -2^N to 2^N-1 $+2^{(N/2)-1}$;--

MAILING ADDRESS OF SENDER

PATENT NO. 6,983,300

James H. Morris
Wolf, Greenfield & Sacks, P.C.
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Boston, Massachusetts 02210

JAN 18 2006